



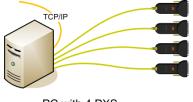
What is it?

The PXS_u is a USB to synchronous adaptor. Connected directly to a computer's USB port or indirectly through a USB hub, the PXS_u can provide synchronous communication just as an internal synchronous adaptor does. Combined with low cost notebooks or PCs and their peripheral devices, the PXS_u can support a wealth of new applications, such as synchronous to TCP/IP or wireless. Synchronous protocols, such as LAPB, LAPD, X.25, Bisynchronous and Monosynchronous are supported through our LayGO multiprotocol host services.

USB the Alternative for PCMCIA and PCI

Nearly all PCs or computers today come with built-in USB and Ethernet ports, supported by the operating systems. Because of the wide use of

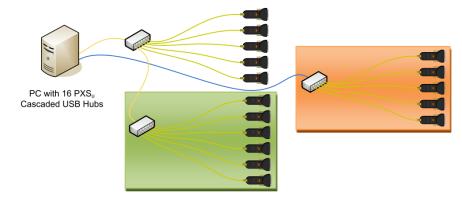




PC with 4 PXS_u

USB, the PXS_u is a true alternative for disappearing Notebook with 2 PXS_u synchronous PCMCIA and PCI adaptors. Few notebooks today still support PCMCIA cards correctly or not at all, and the few are pricy. Current notebooks come at least with 2, PCs with 4 USB ports. Each USB port can be converted by the PXS_u to a synchronous port supporting HDLC protocols such as X.25, LAPB or others. If required, USB hubs can increase the number of synchronous lines available. Newer hubs support high-speed USB (480 Mbps)

to the host computer and can scale down to the speeds of the connected USB devices.



The PXS $_u$, a USB device, receives its power from the USB host (PC, notebook, USB hub). Under full - duplex 4 Mbps sync speed, the PXS $_u$ uses 190 mA, well below the 500 mA maximum. In sleep mode, it uses less than 300 μ A, again, well below the 500 μ A maximum.

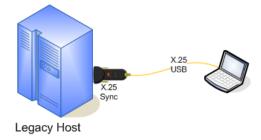
SYNC Ports

The synchronous port uses a built-in DB25 connector, configurable for RS-232, RS-422, RS-485 and V.35. RS-232 supports 128 kbps; RS-422/485 and V.35 support 4.096 Mbps (2xE1). If the PXS_u operates as DCE (clock source), the DB25 connector is X-Over female; as DTE (clock sink), straight male.

The PXS_u supports bit synchronous and byte synchronous modes. Bit synchronous can be bit-transparent or HDLC/SDLC; byte synchronous can be Bisynchronous or Monosynchronous. Data encoding can be NRZ, NRZI, FMO, FM1 or Manchester. Each PXS_u can be independently configured: DTE or DCE, RS-232, RS-422 or V.35, HDLC or Bisynchronous, X.25/LAPB or X.25/LAPD, etc.

What about current LayGO users?

The PXS_u operates exactly as an internal synchronous adaptor. Current users of PCI, PCMCIA, PC/104, PMC and even ISA cards need only replace the existing LayGO API DLL. No changes to existing LayGO applications are necessary.



The PXS_u can be directly connected to a PC's USB port or to a USB hub. The USB host (PC or hub) auto-detects the speed of the PXS_u USB device.

What does it include?

In addition to the PXS_u synchronous adaptor, we provide Lay GO^{\otimes} , our highly modular multiprotocol stack (X.25, LAPB, LAPD, NRM, Frame Relay and proprietary). The combined use of LayGO and host-based TCP/IP or wireless services provides a great variety of communication solutions. Besides HDLC, we support drivers for SDLC, bit transparent, Bisynchronous and Monosynchronous modes.



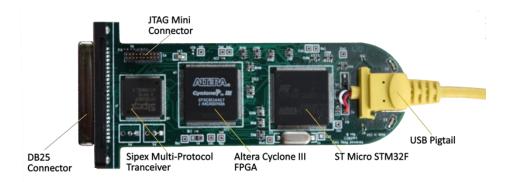
Hardware

The PXS $_u$ is very compact, with built-in DB25 connector (male or female) and a USB pig-tail. The DB25 is the most common connector, used by RS-232, EIA-530 and often by V.35. Normally, the male connector uses thumbscrews, the female hex nuts. If other connectors are required, such as Winchester for V.35, DB15 for X.21 or DB37 for RS-449 (V.36), adaptor cables can be provided. Two programmable LEDs (1 green, 1 red), and 3 states of operation (off, on, blinking) indicate the state of operation of the PXS $_u$.

A powerful feature of the PXS_u is its support for the USB DFU specification, which allows field updates of the firmware and the FPGA net map.

The major PXS_u components are a microprocessor, an FPGA and a programmable I/O chip:

- STMicroelectronics STM32F 32-bit Cortex M3 ARM7 microprocessor, 64 KB SRAM and 512 KB with XIP (eXecute In Place) NOR-Flash and built-in USB device controller.
- Altera Cyclone III EP3C5 FPGA with 5,136 Logic Elements and 414 Kbits RAM.
- SIPEX SPC3508 Multiprotocol Transceiver asynchronous/synchronous serial port.



FPGA

Another powerful feature is provided by the FPGA (Field Programmable Gate Array). Because of incomplete support for synchronous communication by microprocessors, Advanced Relay has developed a class of efficient LayGO/Sync cores using VHDL. The HDLC core uses only 16% of the FPGA's 5,136 logic elements and includes the configuration of the board ID, asynchronous or synchronous port selection, DTE/DCE clock routing and RS-232, RS-422, V.35 signaling mode. The remaining capacity can be used to design custom features in VHDL, such as a 13-bit bound radar protocols, data encryption, data compression, USB-core, wireless protocols, etc.

PXS_u Specifications

Environmental

- Temperature, system on: 0° to 45°C / 32° to 113° F
- Temperature, system off:
 -20° to 85°C / -4° to 185° F
- Humidity, system on: 8% to 80%
- Humidity, system off: 20% to 80%
- Altitude: 0 to 10,000 feet / 0 to 3100 meters
- Heat Output:3.24 BTU/hour / 950 joules/sec
- MTBF: 40.0 years

Regulatory Approvals

FCC, Class A, CE, UL, CUL, C-tick.

Physical

- Dimensions (LxWxH):
 4.69" x 2.37" x .74" / 119mm x 60mm x 19mm
- Weight with Cable:4.5 ounces / 127.6 grams
- Cable Length: 8 feet / 2.4 meters

Power

- Current Consumption:
 200 mA @ 5VDC
- Power Consumption:1 W

Warranty

The PXS_u hardware has a two year warranty.

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